

WHAT IS CLAIMED IS:

1 1. A method of handling memory read return data from different time domains,
2 comprising:
3 determining a number of distinct memory device ranks;
4 determining a time domain for each of the distinct memory device ranks; and
5 scheduling a transaction based on the time domain for each of the distinct
6 memory device ranks so that at least one of data collisions and out-of-order data returns
7 are prevented.

1 2. The method according to claim 1, further including determining a relative position
2 of each of the distinct memory device ranks.

1 3. The method according to claim 1, wherein the determining of the number of the
2 distinct memory device ranks is performed utilizing Serial Presence Detect (SPD).

1 4. The method according to claim 1, wherein the determining of the time domain for
2 each of the distinct memory device ranks includes:
3 writing a predetermined data pattern to a memory device rank to be tested;
4 reading back the predetermined data pattern;
5 receiving the predetermined data pattern, assuming that the time domain of the
6 memory device rank to be tested is in a first time domain;
7 determining whether the predetermined data pattern was correctly received;

8 increasing the time domain of the memory device rank to be tested by at least a
9 clock if the predetermined data pattern was not correctly received; and
10 establishing the time domain for the memory device rank to be tested once the
11 predetermined data pattern is correctly received.

1 5. The method according to claim 1, wherein the scheduling of the transaction
2 includes:

3 determining whether a new request is available;
4 determining whether there are pending or outstanding transactions if the new
5 request is available;
6 consulting a history of pending or outstanding transactions;
7 determining whether a data contention conflict exists;
8 determining whether the data contention conflict may be resolved by scheduling
9 the transaction now and sending the transaction later if the data contention conflict exists;
10 waiting at least a clock if the data contention conflict cannot be resolved by
11 scheduling the transaction now and sending the transaction later;
12 determining whether an out-of-order data conflict exists if the data contention
13 conflict does not exist, and scheduling the transaction if the out-of-order data conflict
14 does not exist; and
15 determining if the out-of-order data conflict exists if the data contention conflict
16 can be resolved by scheduling the transaction now and sending the transaction later, and
17 scheduling the transaction if the out-of-order data conflict does not exist.

- 1 6. The method according to claim 5, further including:
- 2 determining whether out-of-order data conflicts are allowed if the out-of-order
- 3 data conflict exists, and scheduling the transaction if out-of-order data conflicts are
- 4 allowed;
- 5 determining whether the out-of-order data conflict may be resolved by scheduling
- 6 the transaction now and sending the transaction later if out-of-order data conflicts are not
- 7 allowed;
- 8 waiting at least a second clock if the out-of-order data conflict cannot be resolved
- 9 by scheduling the transaction now and sending the transaction later; and
- 10 scheduling the transaction if the out-of-order data conflict may be resolved by
- 11 scheduling the transaction now and sending the transaction later.

- 1 7. The method according to claim 1, wherein the scheduling of the transaction
- 2 includes:
- 3 determining whether a new request is available;
- 4 determining whether there are pending or outstanding transactions if the new
- 5 request is available;
- 6 consulting a history of pending or outstanding transactions;
- 7 determining whether a data contention conflict exists;
- 8 determining whether the data contention conflict may be resolved by scheduling
- 9 the transaction now and sending the transaction later if the data contention conflict exists;
- 10 waiting at least a clock if the data contention conflict cannot be resolved by
- 11 scheduling the transaction now and sending the transaction later;

12 scheduling the transaction if the data contention conflict may be resolved by
13 scheduling the transaction now and sending the transaction later; and
14 scheduling the transaction if the data contention conflict does not exist.

1 8. A memory system, comprising:
2 a plurality of distinct memory device ranks;
3 a memory controller having a connection with the plurality of the distinct memory
4 device ranks, wherein the memory controller is adapted to determine a number of the
5 distinct memory device ranks, to determine a time domain for each of the distinct
6 memory device ranks, and to schedule a transaction based on the time domain for each of
7 the distinct memory device ranks so that at least one of data collisions and out-of-order
8 data returns are prevented.

1 9. The memory system according to claim 8, wherein the memory controller is
2 further adapted to determine a relative position of each of the distinct memory device ranks.

1 10. The memory system according to claim 8, wherein the memory controller utilizes
2 Serial Presence Detect (SPD) to determine the number of the distinct memory device ranks.

1 11. The memory system according to claim 8, wherein the memory controller, in
2 order to determine the time domain for each of the distinct memory device ranks, is adapted to
3 write a predetermined data pattern to a memory device rank to be tested, to read back the
4 predetermined data pattern, to receive the predetermined data pattern assuming that the time

5 domain of the memory device rank to be tested is in a first time domain, to determine whether
6 the predetermined data pattern was correctly received, to increase the time domain of the
7 memory device rank to be tested by at least a clock if the predetermined data pattern was not
8 correctly received, and to establish the time domain for the memory device rank to be tested once
9 the predetermined data pattern is correctly received.

1 12. The memory system according to claim 8, wherein the memory controller, in
2 order to schedule the transaction, is adapted to determine whether a new request is available, to
3 determine whether there are pending or outstanding transactions if the new request is available,
4 to consult a history of pending or outstanding transactions, to determine whether a data
5 contention conflict exists, to determine whether the data contention conflict may be resolved by
6 scheduling the transaction now and sending the transaction later if the data contention conflict
7 exists, waiting at least a clock if the data contention conflict cannot be resolved by scheduling
8 the transaction now and sending the transaction later, to determine if an out-of-order data conflict
9 exists if the data contention conflict does not exist and schedule the transaction if the out-of-
10 order data conflict does not exist, and to determine if the out-of-order data conflict exists if the
11 data contention conflict can be resolved by scheduling the transaction now and sending the
12 transaction later and schedule the transaction if the out-of-order data conflict does not exist.

1 13. The memory system according to claim 12, wherein the memory controller, in
2 order to schedule the transaction, is further adapted to determine whether out-of-order data
3 conflicts are allowed if the out-of-order data conflict exists and schedule the transaction if out-of-
4 order data conflicts are allowed, to determine whether the out-of-order data conflict may be

5 resolved by scheduling the transaction now and sending the transaction later if out-of-order data
6 conflicts are not allowed, to wait at least a second clock if the out-of-order data conflict cannot
7 be resolved by scheduling the transaction now and sending the transaction later, and to schedule
8 the transaction if the out-of-order data conflict may be resolved by scheduling the transaction
9 now and sending the transaction later.

1 14. The memory system according to claim 8, wherein the memory controller, in
2 order to schedule the transaction, is adapted to determine whether a new request is available, to
3 determine whether there are pending or outstanding transactions if the new request is available,
4 to consult a history of pending or outstanding transactions, to determine whether a data
5 contention conflict exists, to determine whether the data contention conflict may be resolved by
6 scheduling the transaction now and sending the transaction later if the data contention conflict
7 exists, waiting at least a clock if the data contention conflict cannot be resolved by scheduling
8 the transaction now and sending the transaction later, to schedule the transaction if the data
9 contention conflict may be resolved by scheduling the transaction now and sending the
10 transaction later, and to schedule the transaction if the data contention conflict does not exist.

1 15. The memory system according to claim 8, wherein the connection is a bus.

1 16. The memory system according to claim 15, wherein the bus includes a data bus
2 and an address/command bus.

1 17. A memory controller, comprising:

2 a machine-readable medium; and
3 machine-readable program code, stored on the machine-readable medium, having
4 instructions to,
5 determine a number of distinct memory device ranks,
6 determine a time domain for each of the distinct memory device ranks,
7 and
8 schedule a transaction based on the time domain for each of the distinct
9 memory device ranks so that at least one of data collisions and out-of-order data
10 returns are prevented.

1 18. The memory controller according to claim 17, wherein the machine-readable
2 program code includes instructions to determine a relative position of each of the distinct
3 memory device ranks.

1 19. The memory controller according to claim 17, wherein the memory controller
2 utilizes Serial Presence Detect (SPD) to determine the number of the distinct memory device
3 ranks.

1 20. The memory controller according to claim 17, wherein the machine-readable
2 program code, to determine the time domain for each of the distinct memory device ranks,
3 includes instructions to:
4 write a predetermined data pattern to a memory device rank to be tested;
5 read back the predetermined data pattern;

6 receive the predetermined data pattern, assuming that the time domain
7 of the memory device rank to be tested is in a first time domain;
8 determine whether the predetermined data pattern was correctly
9 received;
10 increase the time domain of the memory device rank to be tested by at least a
11 clock if the predetermined data pattern was not correctly received; and
12 establish the time domain for the memory device rank to be tested once the
13 predetermined data pattern is correctly received.

1 21. The memory controller according to claim 17, wherein the machine-readable
2 program code, to schedule the transaction, includes instructions to:
3 determine whether a new request is available;
4 determine whether there are pending or outstanding transactions if the new
5 request is available;
6 consult a history of pending or outstanding transactions;
7 determine whether a data contention conflict exists;
8 determine whether the data contention conflict may be resolved by scheduling
9 the transaction now and sending the transaction later if the data contention conflict exists;
10 wait at least a clock if the data contention conflict cannot be resolved by
11 scheduling the transaction now and sending the transaction later;
12 determine if an out-of-order data conflict exists if the data contention conflict
13 does not exist, and scheduling the transaction if the out-of-order data conflict does not
14 exist; and

15 determine whether the out-of-order data conflict exists if the data contention
16 conflict can be resolved by scheduling the transaction now and sending the transaction
17 later, and scheduling the transaction if the out-of-order data conflict does not exist.

1 22. The memory controller according to claim 17, wherein the machine-readable
2 program code, to schedule the transaction, further includes instructions to:

3 determine whether out-of-order data conflicts are allowed if the out-of-order data
4 conflict exists, and scheduling the transaction if out-of-order data conflicts are allowed;

5 determine whether the out-of-order data conflict may be resolved by scheduling
6 the transaction now and sending the transaction later if out-of-order data conflicts are
7 not allowed;

8 wait at least a second clock if the out-of-order data conflict cannot be resolved by
9 scheduling the transaction now and sending the transaction later; and

10 schedule the transaction if the out-of-order data conflict may be resolved by
11 scheduling the transaction now and sending the transaction later.

1 23. The memory controller according to claim 17, wherein the machine-readable
2 program code, to schedule the transaction, includes instructions to:

3 determine whether a new request is available;

4 determine whether there are pending or outstanding transactions if the new
5 request is available;

6 consult a history of pending or outstanding transactions;

7 determine whether a data contention conflict exists;

8 determine whether the data contention conflict may be resolved by scheduling
9 the transaction now and sending the transaction later if the data contention conflict exists;
10 wait at least a clock if the data contention conflict cannot be resolved by
11 scheduling the transaction now and sending the transaction later;
12 schedule the transaction if the data contention conflict may be resolved by
13 scheduling the transaction now and sending the transaction later; and
14 schedule the transaction if the data contention conflict does not exist.